



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Ting-Wah Wong et al.

Serial No.: 10/081,111

Filed: February 21, 2002

For: Integrated Radio
Frequency Circuits

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Art Unit: 2811

Examiner: Ori Nadav

Atty Docket: PSS.0029P7US

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Brief
submitted
8/8/03

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed April 7, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Programmable Silicon Solutions.

II. RELATED APPEALS AND INTERFERENCES

None.

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III. STATUS OF THE CLAIMS

Claims 1-5, 7-10, 20-24, 26, and 31-37 are rejected. Each rejection is appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

Referring to Figure 22, a cascode circuit 310 includes a first transistor 312 coupled to a common gate transistor 314 formed in a triple well. The triple well includes a P-well 320, an N-well 318 and a P-type substrate 316. The drain 336 of the transistor 314 is coupled to the output node 330 and the source 334 is coupled via the line 332 to the drain 336 of the transistor 312. The gates 322 of each transistor 312 or 314 are coupled to a gate node 328. The contacts 332 connect to contact diffusions that are formed in the substrate 316. The lines 332 may be coupled to ground. The wells 318 and 320 of the transistor 314 may be coupled through resistors 324 to biased nodes 326. See specification at page 25, line 22 through page 26, line 25.

The use of the triple well applied to the common gate transistor 314 of the cascode 310 reduces the output shunt capacitance to achieve higher output bandwidth. The well 320 may be a lightly doped P-type well inside a lightly doped N-type well 318. The common gate transistor 314 is placed inside the triple well to reduce the output shunt capacitance by adding two series capacitors from the output drain node 330 of the common gate stage to the substrate node. The two series capacitors are formed by the two triple well P-N junctions, i.e. the junction between the P-well 320 and the N-well 318 and the junction between the N-well 318 and substrate 316. The lightly doped nature of the triple well allows further improvement by reducing the

capacitance of the resulting P-N junctions. Furthermore, the wells 318 and 320 are biased through high value resistors 324 to maintain isolation between the drain node 330 and substrate 316.

Thus, the cascode circuit 310 may be formed in any integrated circuit including those that also include integrated inductors and capacitors, for example to form radio frequency circuits. As a result, the output capacitance is reduced, increasing the available output bandwidth.

Referring next to Figure 23, a plurality of different circuit elements may be formed in a P-type substrate 448, in accordance with one embodiment of the present invention. For example, a complementary metal oxide semiconductor (CMOS) transistor 410 may be formed over a triple well 412 including a P-well 422 and an N-well 420. The NMOS transistor 418 of the CMOS transistor 410 may include sources and drains 430 and 432, and a gate 434. The PMOS transistor 416 may have sources and drains 424 and 426 formed in a P-well 422 and a gate 428. See specification at page 27, line 1 through page 28, line 7.

In one embodiment, the P-well 422 may be biased by a potential V_D through a resistor 427. Similarly, the N-well 420 may be biased by a potential V_A through a resistor 436. The resistors 436 and 427 may have different resistances. The values of those resistances are advantageously greater than 100 ohms and may range from 100 ohms to a few thousand ohms in some embodiments. The potentials V_A and V_D may be the same potential or may be different potentials. In one embodiment, the potentials V_A and V_D may be a supply potential V_{CC} or a ground potential V_{SS} . For example, the potentials V_A and V_D may be supplied through an on-chip pad or connector 460 that may be coupled to a supply voltage V_{CC} via a trace including paths 457 and 459. Alternatively, the potentials V_A and V_D may be supplied through a common trace leading to the pad or connection 462 that may be coupled to V_{SS} .

A plurality of devices formed in the same substrate 448 may all include well bias in one embodiment of the present invention. In some cases, a single supply voltage and a single ground voltage may be applied to the wells of the triple wells of a plurality of different devices. However, by coupling a common bias potential to different wells through suitable resistors, such as the resistors 427 and 436, the amount of noise coupling through common traces may be reduced.

The wells of a triple well may share a common connection through a trace to ground or power supply. The common connection trace has finite inductance and resistance that creates a signal path for noise coupling. The common trace reduces the isolation of triple wells especially at higher frequencies, for example, greater than a few MegaHertz. By the inclusion of the resistors in the bias path, the amount of noise coupling may be reduced. The value of the resistors, such as the resistors 436 and 427, may be larger than the triple well capacitive impedance and small enough to supply bias current to allow a stable voltage for the biased well. See specification at page 28, line 8 through page 29, line 18.

A variety of technologies may be used to form the resistors, such as resistors 436 and 427. For example, polysilicon resistors may be utilized in one embodiment. In another embodiment, diffused resistors may be formed in the substrate 448.

The issue of noise coupling is more acute in connection with radio frequency devices. Radio frequency devices are devices that may be formed in the substrate 448 and operate at frequencies of above one MegaHertz. Examples of radio frequency devices include devices for forming cellular radios, Bluetooth transceivers, conventional radios, and wireless radio frequency networking devices, to mention a few examples.

The substrate 448, in one embodiment, may also include an NMOS transistor 414, having an N-well 438 biased by a potential V_B through a resistor 446. The potential V_B may be the same as one or both of the potentials V_D and the potential V_A in one embodiment of the present invention. The NMOS transistor 414 includes a gate 444. A triple well is formed by the source and drains 440 and 442, the N-well 438 and the P-type substrate 448.

As used herein, the term “triple well” does not encompass a bipolar transistor. Instead, it is intended to refer to the formation of a device in wells of at least three different conductivity types.

As still another example, an integrated inductor, such as a spiral inductor 454 may be formed over the P-type substrate 448 over a triple well including a P-type well or tub 452, and an N-type well 450. A resistor 456 may be coupled to a well bias V_C . As described previously, the potential V_C may be the same or different as any of the other potential supplied through resistors or other devices in the substrate 448. In addition, the P-well 452 may also be biased through a resistor 453 coupled to a potential V_D . Each of the potentials described herein may be a supply potential which is supplied to a plurality of devices in the substrate 448 or a ground potential which is also supplied to a plurality of devices in the substrate 448. See specification at page 29, line 19 through page 31, line 4.

VI. ISSUES

- A. Is Claim 1 Obvious Over Momohara in View of Ng and the Asserted Applicant Admitted Prior Art?**
- B. Is Claim 7 Obvious Over Momohara?**
- C. Is Claim 31 Obvious Over Momohara in View of Ng and the Applicant Admitted Prior Art?**

D. Are Claims 31-37 Indefinite Under Section 112, Second Paragraph?

VII. GROUPING OF THE CLAIMS

Claims 1-5, 8-10, and 20-25 may be grouped.

Claims 7, 10, and 26 may be grouped.

Claims 31-37 may be grouped.

VIII. ARGUMENT

A. Is Claim 1 Obvious Over Momohara in View of Ng and the Asserted Applicant Admitted Prior Art?

Claim 1 calls for a method including forming a metal oxide semiconductor radio frequency circuit element over a triple well in a substrate and biasing a well of the triple well through a resistor. As explained in the specification, a triple well is a type of substrate structure utilized in metal oxide semiconductor circuits. It includes a plurality of doped regions of different conductivity types.

With the resistor bias and a MOS circuit element positioned over the triple well operating in the radio frequency range, the AC characteristics of the circuit are improved. Namely, referring to Figure 22, a resistor 324 is coupled from supply to an N-well 318, inside a triple well, on a P-type substrate 316. For RF frequencies, the resistor 324 acts as a high impedance relative to the junction capacitance of the N-well 318 to P-well 320 junction. Then a MOSFET 314 over the P-well 320 sees less loading through this well junction capacitance when that capacitance is in series with the resistor 324. A similar point can be made where the resistor is coupled to the P-well.

Thus, it is the AC characteristics of the circuit that are improved in the case of radio frequency circuit elements as claimed and it is not just the simple biasing through a resistor.

Nothing in any of the references cited in any way suggest the advantages that can be achieved at radio frequencies using resistor bias. Therefore the invention should patentably distinguish over all of these references.

As explained on page 27 of the present application, use of the triple well applied to the common gate transistor 314 of the cascode circuit 310 reduces the output shunt capacitance to achieve higher output bandwidth. It is explained at the bottom of page 29 and the top of page 30 that noise coupling is more acute in connection with radio frequency devices and that radio frequency devices are devices that operate at frequencies above 1 MegaHertz.

Therefore, the rejection of claim 1 should be reversed.

B. Is Claim 7 Obvious Over Momohara?

In the office action, it is claimed that claim 7 is somehow obvious over Momohara because it would be obvious to provide whatever resistor is needed to achieve the desired bias potential.

Of course, the problem with this argument is that Momohara does not even teach using a resistor to apply the bias. Moreover, Momohara does not teach any reason to use a resistor higher than 100 ohms. It is unlikely that a resistor this size would be utilized for biasing. Instead, use of a resistor at this size is to improve the AC characteristics.

Since there is no teaching to modify Momohara to provide a resistor bias, no teaching to use a resistor greater than 100 ohms and no rationale to modify the reference to achieve this result, the rejection should be reversed.

C. Is Claim 31 Obvious Over Momohara in View of Ng and the Applicant Admitted Prior Art?

Claim 31, *inter alia*, calls for providing a high impedance resistor to bias a well of a triple well. The high impedance is high relative to the junction capacitance within the triple well.

There is no teaching of using any kind of impedance in the biasing path to a well. Moreover, there is no teaching that that impedance should be high relative to a given capacitance. Absent any teaching or any rationale to make the claimed invention, the rejection is plainly without merit and should be reversed.

D. Are Claims 31-37 Indefinite Under Section 112, Second Paragraph?

Claims 31-37 have rejected as being indefinite because the claims recite that the resistor acts as a high impedance relative to the junction capacitance within the triple well.

The Examiner suggests that it is unclear how an impedance can be compared to another impedance in the form of a capacitance. This is a basic tenet of electrical engineering, which permits different impedances to be compared. Therefore, one skilled in the art would have no trouble understanding how the resistor may be compared to the impedance of a capacitance.

In particular, in the impedance Z_R of a resistor is its resistance, while the impedance of a capacitance is $1/j\omega C$. See e.g., the basic primer "Introduction to Modern Circuit Analysis," Calahan et al. (1974) at pages 234-235 (copy attached).

Therefore, the rejection of claims 31-37 under Section 112 should be reversed.

IX. CONCLUSION

Applicants respectfully request that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: July 18, 2003



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APPENDIX OF CLAIMS

The claims on appeal are:

1. A method comprising:
forming a metal oxide semiconductor radio frequency circuit element over a triple well in a substrate; and
biasing a well of said triple well through a resistor.
2. The method of claim 1 including forming an integrated inductor over a triple well.
3. The method of claim 1 including forming a P-type well in an N-type well formed in said substrate.
4. The method of claim 3 including biasing the N-type and P-type wells through different resistors.
5. The method of claim 1 including providing a common bias potential to different wells through separate resistors for each well.
7. The method of claim 5 including biasing said wells through resistors having a resistance greater than one hundred ohms.

8. The method of claim 7 including forming a complementary metal oxide semiconductor transistor over a triple well and biasing at least one of the wells of said triple well through a resistor.

9. The method of claim 1 including forming a plurality of triple wells in said substrate and forming a circuit element over each of said triple wells, biasing at least one well of each of said triple wells through a common potential, each of said potentials being applied to said wells through a resistor.

10. The method of claim 9 including applying a supply potential to said plurality of wells through a resistor.

20. A method comprising:

- forming a first metal oxide semiconductor radio frequency circuit element over a triple well in a substrate;
- biasing a first well of said triple well through a first resistor with a first bias potential;
- forming a second metal oxide semiconductor radio frequency circuit element over a second triple well in a substrate; and
- biasing a second well of said second triple well through a second resistor coupled to said first bias potential.

21. The method of claim 20 including coupling the first bias potential to said first and second wells through a common trace to a supply potential.

22. The method of claim 20 including forming an integrated inductor over the first triple well.

23. The method of claim 20 including forming a P-type well and an N-type well formed in said substrate.

24. The method of claim 23 including biasing the N-type and P-type wells through different resistors.

26. The method of claim 20 including biasing said wells through resistors having a resistance greater than 100 ohms.

31. A method comprising:
forming a metal oxide semiconductor circuit element over a triple well in a substrate;
operating said circuit element at a radio frequency; and
biasing a well of said triple well through a resistor which acts as a high impedance relative to a junction capacitance within the triple well.

32. The method of claim 31 including forming an integrated inductor over said triple well.

33. The method of claim 31 including forming a P-type well in an N-well formed in said substrate.

34. The method of claim 33 including biasing the N-type and P-type wells through different resistors.

35. A method of claim 31 including providing a common bias potential to different wells through separate resistors for each well.

36. The method of claim 35 including biasing said wells through resistors having a resistance greater than 100 ohms.

37. The method of claim 31 including coupling a resistor to an N-well within said triple well on a P-type substrate so that said resistor acts as a high impedance relative to the junction capacitance of the N-well to the P-well of the triple well.